PL-IC-MH Datasheet
Issue 5, Oct 24, 2014

Magnetic encoder module and Magnetic actuator

PL-IC-MH Magnetic encoder module

Magnetic Actuator

1. General Description

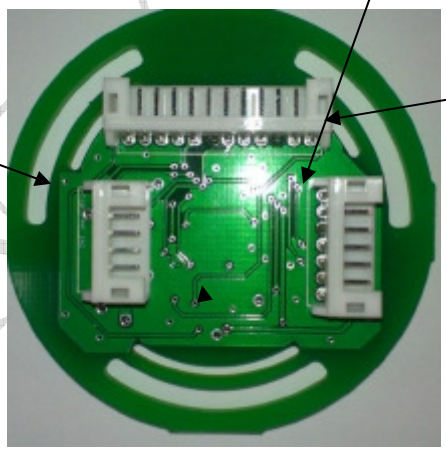
The PL-IC-MH encoder module is designed for easy installation with a self aligning metal mounting flange. The low cost module can be provided with an integrated connector. The encoder module consists of a magnetic actuator and a separate sensor board. An internal voltage regulator allows the PL-IC-MH to operate at either 5 V supplies.

The PL-IC-MH module can be used in a wide range of applications including motor control and industrial automation.

2. Pin Configuration

Pin 7 NC
Pin 6 NC
Pin 5 NC
Pin 4 NC
Pin 3 W
Pin 2 V
Pin 1 U

Pin 6 DO
Pin 5 CSN
Pin 4 CLK
Pin 3 Vzap
Pin 2 GND
Pin 1 5V



Pin12-5V
Pin11-0V
Pin10-B+
Pin 9-B-
Pin 8-A+
Pin 7-A-
Pin 6-Do
Pin 5-CLK
Pin 4-CSN
Pin 3-NC
Pin 2-Z-
Pin 1-Z+

3. ELECTRICAL CHARACTERISTICS

Operating conditions:
VPA, VPD = 5V ±10 %, Tj = -40...125°C, IBM adjusted to 200µA , 4 mm NdFeB magnet, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	V(VPA, VPD)	Supply Voltage Range		4.5		5.5	V
002	I(VPA)	Supply Current in VPA		3		8	mA
003	I(VPD)	Supply Current in VPD	PRM = '0', without Load	5		15	mA
004	I(VPD)	Supply Current in VPD	PRM = '1', without Load	2		10	mA
005	Vc(hi)	Clamp Voltage hi at MA, SLI, SLO, PTE, NERR	Vc()hi = V() – VPD, I() = 1 mA	0.4		1.5	V
006	Vc(lo)	Clamp Voltage lo	I() = -1 mA	-1.5		-0.3	V
Hall Sensors and Signal Conditioning							
101	Hext	Operating Magnetic Field Strength	At Chip Surface	20		100	kA/m
102	fmag	Operating Magnetic Field Frequency Rotating Speed of Magnet				2 120 000	kHz rpm
103	dsens	Diameter of HALL Sensor Array			2		mm
104	xdis	Lateral Displacement of Magnet to Chip				0.2	mm
105	xpac	Displacement Chip to Package	QFN28 package	-0.2		0.2	mm
106	ϕpac	Angular alignment of chip vs. package	QFN28 package	-3		+3	Deg
107	hpac	Distance of chip surface to package surface	QFN28 package		0.4		mm
108	Vos	Trimming range of output offset voltage	VOSS or VOSC = 0x7F			-55	mV
109	Vos	Trimming range of output offset voltage	VOSS or VOSC = 0x3F	55			mV
110	Vopt	Optimal differential output voltage	Vopt = Vpp(PSIN) – Vpp(NSIN), ENAC = '0', see Fig. 6		4		Vpp
Amplitude Control							
201	Vampl	Differential Output Amplitude	Vampl = Vpp(PSIN) – Vpp(NSIN), ENAC = '1', see Fig. 6	3.2		4.8	Vpp
202	Vratio	Amplitude Ratio	Vratio = Vpp(PSIN) / Vpp(PCOS)	1.09			
203	Vratio	Amplitude Ratio	Vratio = Vpp(PSIN) / Vpp(PCOS)			0.91	
204	tampl	Settling Time of Amplitude Control	±10%			300	µs
205	Vae()lo	Amplitude Error Threshold for MINERR	Vpp(PSIN) – Vpp(NSIN)	1.2		2.8	Vpp
206	Vae()hi	Amplitude Error Threshold for MAXERR	Vpp(PSIN) – Vpp(NSIN)	5.0		5.8	Vpp
Bandgap Reference							
401	Vbg	Bandgap Reference Voltage		1.2	1.25	1.3	V
402	Vref	Reference Voltage		45	50	55	%VPA
403	Ibm	Bias Current	CIBM = 0x0 CIBM = 0xF Bias Current adjusted	 -370 -220	 -200	-100 -180	µA µA µA
404	VPDon	Turn-on Threshold VPD, System on	V(VPD) – V(VND), increasing voltage	3.7	4.0	4.3	V
405	VPDoff	Turn-off Threshold VPD, System reset	V(VPD) – V(VND), decreasing voltage	3	3.5	3.8	V
406	VPDhys	Hysteresis System on/reset		0.35			V
407	Vosr	Reference voltage offset compensation		480	500	520	mV

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Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Clock Generation							
501	f()sys	System Clock	Bias Current adjusted	0.85	1.0	1.15	MHz
502	f()sdc	Sinus/Digital-Converter Clock	Bias Current adjusted	14	16	18	MHz
Sin/Digital Converter							
601	RESsdc	Sinus/Digital-Converter Resolution			12		Bit
602	AAabs	Absolute Angular Accuracy	Vpp() = 4 V, adjusted	-0.35		0.35	Deg
603	AArel	Relative Angular Accuracy	with reference to one output periode at A, B, at Resolution 1024, see Fig. 17	-10		10	%
604	f()ab	Output frequency at A, B	CFGMTB = '0' CFGMTB = '1'		0.5 2.0		MHz MHz
605	REScom	Resolution of Commutation Converter			1.875		Deg
606	AAabs	Absolute Angular Accuracy of Commutation Converter		-0.5		0.5	Deg
Serial Interface, Digital Outputs MA, SLO, SLI							
701	Vs(SLO)hi	Saturation Voltage High	V(SLO) = V(VPD) – V(), I(SLO) = 4 mA			0.4	V
702	Vs(SLO)lo	Saturation Voltage Low	I(SLO) = 4 mA to VND			0.4	V
703	Isc(SLO)hi	Short-Circuit Current High	V(SLO) = V(VND), 25°C	-80	-50		mA
704	Isc(SLO)lo	Short-Circuit Current Low	V(SLO) = V(VPD), 25°C		50	80	mA
705	tr(SLO)	Rise Time SLO	CL = 50 pF			60	ns
706	tf(SLO)	Fall Time SLO	CL = 50 pF			60	ns
707	Vt()hi	Threshold Voltage High: MA, SLI				2	V
708	Vt()lo	Threshold Voltage Low: MA, SLI		0.8			V
709	Vt()hys	Threshold Hysteresis: MA, SLI		150	250		mV
710	Ipd(SLI)	Pull-up Current: MA, SLI	V() = 0...VPD – 1 V	6	30	60	µA
711	Ipu(MA)			-60	-30	-6	µA
712	f()MA					10	MHz
Zapping and Test							
801	Vt()hi	Threshold Voltage High VZAP, PTE	with reference to VND			2	V
802	Vt()lo	Threshold Voltage Low VZAP, PTE	with reference to VND	0.8			V
803	Vt()hys	Hysteresis	Vt()hys = Vt()hi – Vt()lo	150	250		mV
804	Vt()nozap	Threshold Voltage Nozap VZAP	V() = V(VZAP) – V(VPD), V(VPD) = 5 V ±5 %, at chip temperature 27 °C	0.8			V
805	Vt()zap	Threshold Voltage Zap VZAP	V() = V(VZAP) – V(VPD), V(VPD) = 5 V ±5 %, at chip temperature 27 °C			1.2	V
806	V()zap	Zapping voltage	PROG = '1'	6.9	7.0	7.1	V
807	V()zpd	Diode voltage, zapped				2	V
808	V()uzpd	Diode voltage, unzapped		3			V
809	Rpd()VZAP	Pull-Down Resistor at VZAP		30		55	kΩ
NERR Output							
901	Vt()hi	Input Threshold Voltage High	with reference to VND			2	V
902	Vs()lo	Saturation Voltage Low	I() = 4 mA , with reference to VND			0.4	V
903	Vt()lo	Input Threshold Voltage Low	with reference to VND	0.8			V
904	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi – Vt()lo	150	250		mV
905	Ipu(NERR)	Pull-up Current	V(NERR) = 0...VPD – 1 V	-700	-300	-60	µA
906	Isc()lo	Short circuit current NERR	V(NERR) = V(VPD), 25°C		50	80	mA
907	tf(NERR)	Decay time NERR	CL = 50 pF			60	ns

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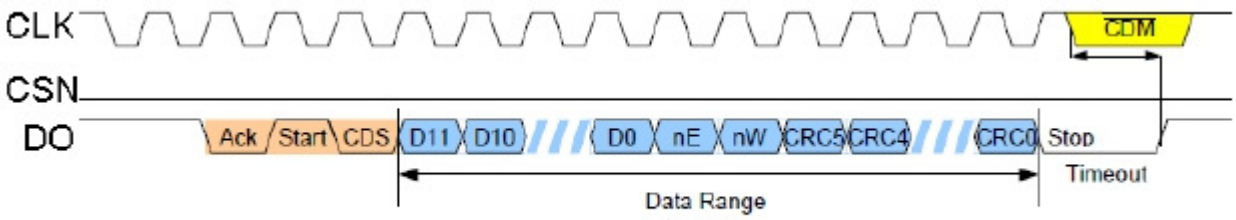
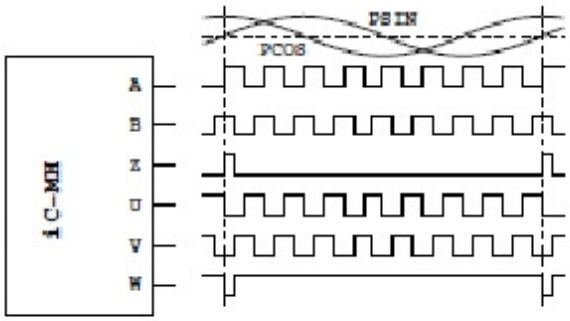
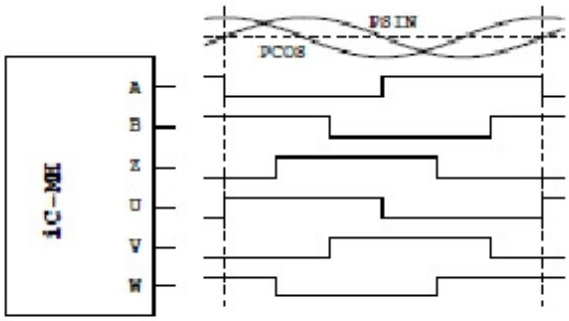
Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Line Driver Outputs							
P01	Vs()hi	Saturation Voltage hi	Vs() = VPD – V(); CfgDR(1:0) = 00, I() = -4 mA CfgDR(1:0) = 01, I() = -50 mA CfgDR(1:0) = 10, I() = -50 mA CfgDR(1:0) = 11, I() = -20 mA			 200 700 700 400	 mV mV mV mV
P02	Vs()lo	Saturation Voltage lo	CfgDR(1:0) = 00, I() = -4 mA CfgDR(1:0) = 01, I() = -50 mA CfgDR(1:0) = 10, I() = -50 mA CfgDR(1:0) = 11, I() = -20 mA			200 700 700 400	mV mV mV mV
P03	Isc()hi	Short-Circuit Current hi	V() = 0 V; CfgDR(1:0) = 00 CfgDR(1:0) = 01 CfgDR(1:0) = 10 CfgDR(1:0) = 11	 -12 -120 -120 -60		 -4 -50 -50 -20	 mA mA mA mA
P04	Isc()lo	Short-Circuit Current lo	V() = VPD; CfgDR(1:0) = 00 CfgDR(1:0) = 01 CfgDR(1:0) = 10 CfgDR(1:0) = 11	 4 50 50 20		 12 120 120 60	 mA mA mA mA
P05	Ilk()tri	Leakage Current Tristate	TRIHL(1:0) = 11	-100		100	µA
P06	tr()	Rise-Time lo to hi at Q	RL = 100 Ω to VND; CfgDR(1:0) = 00 CfgDR(1:0) = 01 CfgDR(1:0) = 10 CfgDR(1:0) = 11	 5 5 50 5		 20 20 350 40	 ns ns ns ns
P07	tf()	Fall-Time hi to lo at Q	RL = 100 Ω to VND; CfgDR(1:0) = 00 CfgDR(1:0) = 01 CfgDR(1:0) = 10 CfgDR(1:0) = 11	 5 5 50 5		 20 20 350 40	 ns ns ns ns



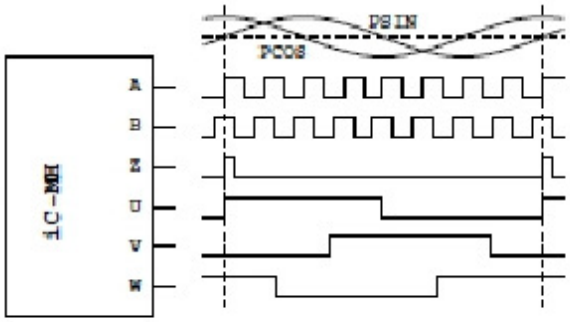
Serial Interface Protocol



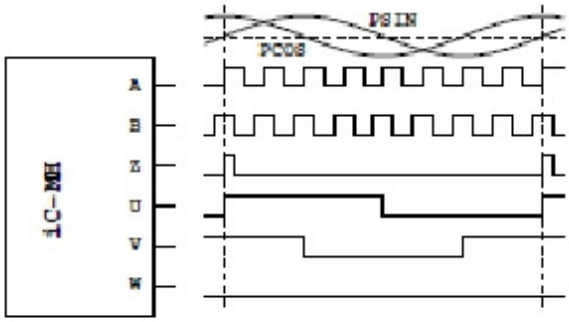
ABZ differential incremental signals



UVW differential commutation signals



ABZ incremental / UVW commutation signals



ABZ incremental signals / period counter

6. Package Drawings & Magnetic Actuator